CLAIMS

1. A coprocessor circuit for processing image data in digital form, including:

a motion vector controller block for generating, starting from said image data, motion vector values including predictor data and macroblock data relating to a current macroblock of said image data to be estimated, said prediction data and macroblock data being adapted to be stored at respective memory addresses,

an address generator block for extracting said respective addresses from said motion vector values,

a predictor fetch block for retrieving said predictor data based on respective addresses extracted by said address generator block,

a current macroblock fetch and distengine block for retrieving said macroblock data based on respective addresses extracted by said address generator block and for processing said macroblock data according to a given function, and

a decision block for collecting said retrieved data as partial results and selecting the best result therefrom.

2. The circuit according to claim 1 wherein said motion vector controller block is implemented as a DSP.

3. The circuit according to claim 1 wherein said motion vector controller block is arranged to run a microcode.

4. The circuit according to claim 3 wherein said motion vector controller block has associated therewith a memory, preferably of the flash type, for storing said microcode.

5. The circuit according to claim 1 wherein said circuit is arranged to perform two distinct estimation steps, namely a coarse search and a fine search, respectively, of said image data, said estimation steps being carried out in parallel on different macroblocks.

6. The circuit according to claim 5 wherein the circuit includes time-sharing hardware resources to generate in parallel the result of the coarse search for a macroblock and the result of the fine search for another macroblock.

7. The circuit according to claim 1 wherein the circuit includes temporal noise reduction means attached at the output of the decision block to noise-reduce said image data.

8. The circuit according to claim 5 wherein said noise reduction means perform motion compensated noise level detection and reduction based on the motion vectors resulting from the coarse search, preferably by using as inputs the coarse search current macroblock and its predictor block.

9. The circuit according to claim 8 wherein said noise reduction means output a noise-reduced version of the current macroblock that will overwrite the noise corrupted one.

10. The circuit according to claim 1 wherein said motion vector controller block is arranged to perform at least one ancillary function selected from the group consisting of scene change detection, inverse 3/2 pull down, interlace/progressive content detection, f_code adaptation.

11. The circuit according to claim 1 wherein said motion vector controller block is arranged to perform at least one function selected from the group consisting of counting the cycles spent to estimate the current macroblock, inserting stall or power down cycles or additional motion vector tests to ensure synchronization with input data.

12. The circuit according to claim 1 wherein said motion vector controller block includes a local memory adapted to receive slices of said motion vectors.

13. The circuit according to claim 12 wherein said motion vector controller block has associated therewith slice FIFOs of a first type containing motion vector data resulting from previous estimation of the macroblock in the same frame and of a second type containing results from estimations of macroblocks in previous pictures or previous passes of prediction.

14. The circuit according to claim 1 wherein said address generator block is arranged to output the addresses required to fetch said predictor data in sequential cycles.

15. The circuit according to claim 1 wherein said address generator block is arranged to issue as voids at least some of said addresses not requiring loading when the absolute coordinates of the predictors are block aligned.

16. The circuit according to claim 1 wherein said predictor fetch block has associated therewith an internal memory managed as a cache memory.

17. The circuit according to claim 16 wherein said predictor fetch block loads the search windows pixels of said image data selectively and/or buffers them in said internal memory by dynamic allocation.

18. The circuit according to claim 14 wherein said predictor fetch block has a bus access limiter coupled to the cache refill engine.

19. The circuit according to claim 18 wherein said bus access limiter is arranged for clipping high-bandwidth peaks.

20. The circuit according to claim 18 wherein said bus access limiter acts at a macroblock by macroblock level.

21. The circuit according to claim 18 wherein said bus access limiter has a selectively variable maximum allowed bandwidth value.

22. The circuit according to claim 16 wherein said cache memory is organized as a multiway, preferably as a 4-way set associative memory.

23. The circuit according to claim 22 wherein said predictor fetch block is arranged to permit selective reading of blocks in each line of said cache memory, thereby permitting all the bytes of each block or only the blocks belonging to one field to be selectively read.

24. The circuit according to claim 16 wherein said cache memory is arranged in order to permit writing of data therein only when refilling the respective refill engine.

25. The circuit according to claim 16 wherein within said cache memory tag lookup and access operations are performed sequentially in subsequent clock cycles.

26. The circuit according to claim 16 wherein said cache memory is physically composed of a single piece instead of N, where N is the number of ways in which said cache is logically organized.

27. The circuit according to claim 16 wherein the circuit includes an intermediate buffer to decouple the tag lookup task from memory access in said cache memory.

28. The circuit according to claim 16 wherein said cache memory is arranged, preferably at the refill engine level, to find in advance the next miss and proceed to pre-load the block from memory.

29. The circuit according to claim 27 wherein, at the first miss, the cache memory access stalls, but tag lookup continues to determine the next miss, preferably by taking care of the tags configuration after that refill.

30. The circuit according to claim 1 wherein said predictor fetch block has associated therewith a predictor alignment block to reformat a block-based output of said predictor fetch block into a lines-of-macroblock output and selecting a sub-array out of the original array or the output of said predictor fetch block.

31. The circuit according to claim 30 wherein said predictor alignment block includes a respective buffer filled by said predictor fetch block.

32. The circuit according to claim 30 wherein said predictor alignment block is arranged to perform interpolation of the data transferred from said predictor fetch block towards said fetch and distengine block.

33. The circuit according to claim 1 wherein said fetch and distengine block applies, as said given function, the mean absolute error over a given macroblock of the sum of absolute differences produced by pixel comparison.

34. The circuit according to claim 23 wherein said fetch and distengine block is arranged as a monodimensional array of computing elements.

35. The circuit according to claim 33 wherein said monodimensional array is a monodimensional array of SAD elements.

36. The circuit according to claim 5 wherein said fetch and distengine block includes a macroblock buffer to store coarse search macroblocks in order to permit processing each macroblock as soon as the coarse search finishes.

37. The circuit according to claim 36 wherein said macroblock buffer is implemented as single ported memory.

38. The circuit according to claim 1 wherein said fetch and distengine block includes a programmable distengine module for field or frame matching.

39. The circuit according to claim 1 wherein said decision block includes a first module to gather the partial result of current block estimation and a second module to compute the macroblock coding decision functions on the motion estimation winner.

40. The circuit according to claim 39 wherein the circuit includes a decision memory, preferably a RAM, to store the winner for each prediction mode.

41. The circuit according to claim 1 wherein the decision block is arranged to compare new data obtained by applying said given function with a current winner for the mode to which the predictor belongs and if the current winner is less than or equal the new data, the new data will replace the current winner.

42. The circuit according to claim 1 wherein said decision block performs decision of the macroblock coding type sequentially or in parallel with respect to motion estimation.

43. The circuit according to claim 42 wherein said decision of the macroblock coding type is performed sequentially with respect to motion estimation and in that the issue of motion vectors is stopped to allow the mode winners memory to be accessed.

44. The circuit according to claim 1 wherein the circuit is formed on a monolithic integrated circuit substrate.

45. A method for processing an image data in digital form comprising:

generating motion vector values including predictor data and macroblock data from input image data to be estimated;

extracting respective addresses from said motion vector values;

retrieving said predictor data based on respective addresses extracted from the motion vector values;

retrieving said macroblock data based on respective addresses extracted from said motion vector values; and

collecting said retrieved macroblock data as partial results and selecting from said partial results a preferred data set.

46. The method according to claim 45 wherein said generating step includes:

performing a coarse search on said image data to perform a first estimation step; and

performing a fine search on the same image data to perform a second estimation step.

47. The method according to claim 46, further comprising:

performing motion compensated noise level detection; and

reducing the noise level based on the motion vectors resulting from the coarse search.

48. The method according to claim 45, further including:

outputting the addresses required to fetch said predictor data in sequential cycles.

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49. The method according to claim 14, further including:

issuing as voids at least some of the addresses not requiring loading when the absolute coordinates of the predictor block are aligned.

50. The method according to claim 45, further including:

continuing to perform tag lookups to determine the next miss when the cache memory access stalls.